IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 09/541,413
Priority Filing Date ..... March 31, 2000
Inventor ..... Neal Margulis
Priority Group Art Unit 2671
Priority Examiner ..... Ulka J. Chauhan
Attorney's Docket No. MA74-012
Title: Computer System Controller Having Internal Memory and External Memory Control

RESPONSE TO MARCH 20, 2002 FINAL OFFICE ACTION
PRELIMINARY AMENDMENT TO ACCOMPANY
CONTINUATION APPLICATION FILING

To: Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

From: Frederick M. Fliegel, Ph.D.
(Tel. 509-624-4276; Fax 509-838-3424)
Wells St. John P.S.
601 West First Avenue, Suite 1300
Spokane, WA 99201-3828

This is a preliminary amendment accompanying a Request for Continuation Application for the above-entitled patent application. Prior to examining the application, please enter the following amendments.

AMENDMENTS

In the Specification

Please replace the paragraph on page 1, immediately following the heading "RELATED APPLICATIONS" with the following clean replacement paragraph:

This patent application is a continuation application of U.S. Patent Application Serial No. 09/541,413, filed on March 31, 2000, entitled "Computer System Controller Having Internal Memory and External Memory Control," naming Neal Margulis as inventor, which is a continuation application of U.S. Patent Application Serial No. 08/926,666, filed on September 9, 1997, now U.S. Patent No. 6,118,462, which resulted from a continuation-in-part application of U.S. Patent Application Serial No. 08/886,237, filed on July 1, 1997, entitled "Computer System Having a Common Display Memory and Main Memory," naming Neal Margulis as inventor, now U.S. Patent No. 6,057,862, the disclosures of which are incorporated by reference.

In the Claims

Please amend the claims as follows:

Cancel claims 1-33 without prejudice.

New Claims

34. A computer system comprising:

a memory controller;

a common display memory and main memory comprising at least one internal memory subsystem contained in the memory controller and at least one external memory subsystem outside of the memory controller;

at least one multi-use memory channel operatively coupled to the at least one internal memory subsystem and the at least one external memory subsystem;

a memory channel data switch coupled to the memory controller and configured to dynamically allocate the at least one multi-use memory channel; and

a central processing unit (CPU) subsystem controller operably coupled to the memory channel data switch and the memory controller, the CPU configured to output control signals to the memory channel data switch and the memory controller.

35. The computer system of claim 34 further comprising a multiplexer configured to selectively couple at least one external memory subsystem to one of the at least one multi-use memory channels.

36. The computer system of claim 34 wherein one of the at least one internal memory subsystem and the at least one external memory subsystem is a display memory subsystem configured to be able to function as main system memory.

37. The computer system of claim 34 wherein at least one of the at least one internal memory subsystem and the at least one external memory subsystem includes a data manipulator containing a plurality of data storage elements.

38. The computer system of claim 34 further comprising a complete drawing buffer configured to permit a graphics engine to store display output data and transfer the display output data for subsequent display updates.

39. The computer system of claim 34 further comprising a computer display, a complete drawing buffer and a graphics engine, wherein the graphics engine is configured to be able to store output data in the drawing buffer for output to the computer display and to subsequently transfer the output data to the computer display for display updates.

40. A computer system comprising:

a display;

a memory controller;

common display memory and main memory comprising at least one of an internal memory subsystem included within the memory controller and configured to cooperatively couple therewith, and at least one of an external memory subsystem outside of the memory controller and configured to cooperatively couple therewith;

a plurality of memory channels operatively coupled to the common display memory and main memory, at least one of the plurality of memory channels configured as a multi-use memory channel;

a memory channel data switch operably coupled to the memory controller and to the plurality of memory channels and configured to allocate selected ones of the plurality of memory channels between the at least one internal memory subsystem and the at least one external memory subsystem;

a central processing unit (CPU) subsystem controller operably coupled to the memory channel data switch and the memory controller and configured to produce output signals to be applied to the memory channel data switch and memory controller;

a graphics/drawing and display subsystem operably coupled to the CPU subsystem controller, the memory channel data switch and the memory controller, the graphics/drawing and display subsystem being configured to

provide output signals to the memory channel data switch and the memory controller;

an arbitration and control engine operably coupled to the CPU subsystem controller, the graphics/drawing and display subsystem, the arbitration and control engine being configured to provide output signals to the CPU subsystem controller and to the graphics/drawing and display subsystem; and

a peripheral bus controller operably coupled to the memory channel data switch, the memory controller and the arbitration and control engine and configured to provide output signals to the memory channel data switch, the memory controller and the arbitration and control engine.

41. The computer system of claim 40 wherein at least one of the at least one internal memory subsystem and the at least one external memory subsystem includes DRAM memory.

42. The computer system of claim 40 wherein at least one of the at least one internal memory subsystem and the at least one external memory subsystem comprises a data manipulator containing a plurality of storage elements.

43. The computer system of claim 40 further comprising a computer display, a complete drawing buffer and a graphics engine, wherein the graphics engine can store output data in the drawing buffer for output to the computer display and subsequently transfer the output data to the computer display for display updates.

REMARKS

Claims 1-33 have been canceled and claims 34-43 have been added. Claims 34-43 remain in the application. Consideration of the application as amended is requested.

New claims 34-43 are supported at least by text appearing at p. 7, line 11 through p. 24, line 18 of the application as originally filed. No new matter is added by new claims 34-43. New claims 34-43 distinguish over the art of record and are allowable.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page(s) are captioned "**Version with markings to show changes made**."

In view of the foregoing, allowance of claims 34-43 is requested. The Examiner is requested to phone the undersigned in the event that the next Office Action is one other than a Notice of Allowance. The undersigned is available for telephone consultation at any time during normal business hours (Pacific Time Zone).

Respectfully submitted,

Dated: Nov. 26, 2002 By: _____

Frederick M. Fliegel, Ph.D.
Reg. No. 36,138

Version with markings to show changes made

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 09/541,413
Priority Filing Date ..... March 31, 2000
Inventor ..... Neal Margulis
Priority Group Art Unit 2671
Priority Examiner ..... Ulka J. Chauhan
Attorney's Docket No. MA74-012
Title: Computer System Controller Having Internal Memory and External Memory Control

VERSION WITH MARKINGS TO SHOW CHANGES MADE TO ACCOMPANY PRELIMINARY AMENDMENT

Deletions are bracketed, additions are underlined.

In the Specification

The paragraph on page 1, immediately following the heading "RELATED APPLICATIONS" has been replaced with the following paragraph:

This patent application is a continuation application of U.S. Patent Application Serial No. 09/541,413, filed on March 31, 2000, entitled "Computer System Controller Having Internal Memory and External Memory Control," naming Neal Margulis as inventor, which is a continuation application of U.S. Patent Application Serial No. 08/926,666, filed on September 9, 1997, now U.S. Patent No. 6,118,462, which resulted from a continuation-in-part application of U.S. Patent Application Serial No. 08/886,237, filed on July 1, 1997, entitled "Computer System Having a Common Display Memory and Main Memory," naming Neal Margulis as

inventor, now U.S. Patent No. 6,057,862, the disclosures of which are incorporated by reference.

In the Claims

Claims 1-33 have been canceled without prejudice and claims 34-43 have been added.

Because the amendments to the claims merely cancel some claims and add others, no marked-up copies of claim amendments are required or provided.

END OF DOCUMENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 09/541,413
Priority Filing Date . . . . . March 31, 2000
Inventor . . . . . Neal Margulis
Priority Group Art Unit 2671
Priority Examiner . . . . . Ulka J. Chauhan
Attorney's Docket No. MA74-012
TITLE: Computer System Controller Having Internal Memory and External Memory Control

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Assistant Commissioner for Patents
Washington, D. C. 20231
Attention: Official Draftsman

SUBSTITUTE DRAWING REQUEST

Please enter the enclosed substitute formal drawings in the above-referenced application in place of drawings originally filed. The content of the drawings are identical to those now on file in this application.

Acknowledgment of receipt of the formal drawings and their acceptance into the file is requested.

Respectfully submitted,

Date: NOV. 20, 2002

By: _____

Frederick M. Fliegel, Ph.D.
Reg. No.: 36,138
WELLS ST. JOHN P.S.
601 W. First Avenue, Suite 1300
Spokane, WA 99201-3828
(509) 624-4276

Enclosures: 12 Sheets of Formal Drawings, Figs. 1-12.

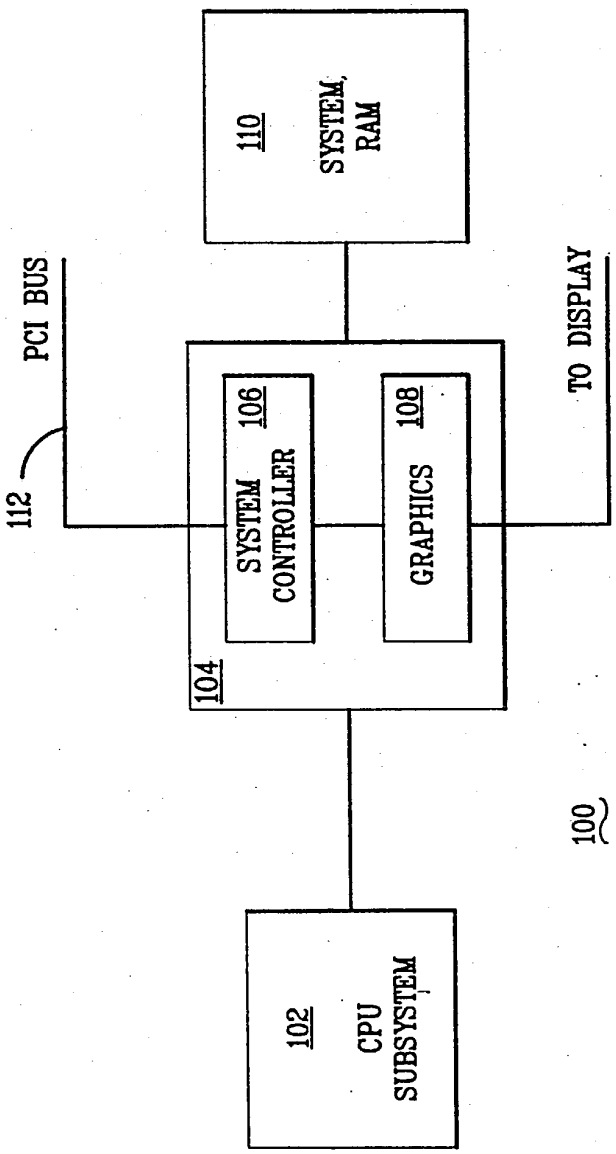

FIG. 1
Prior Art

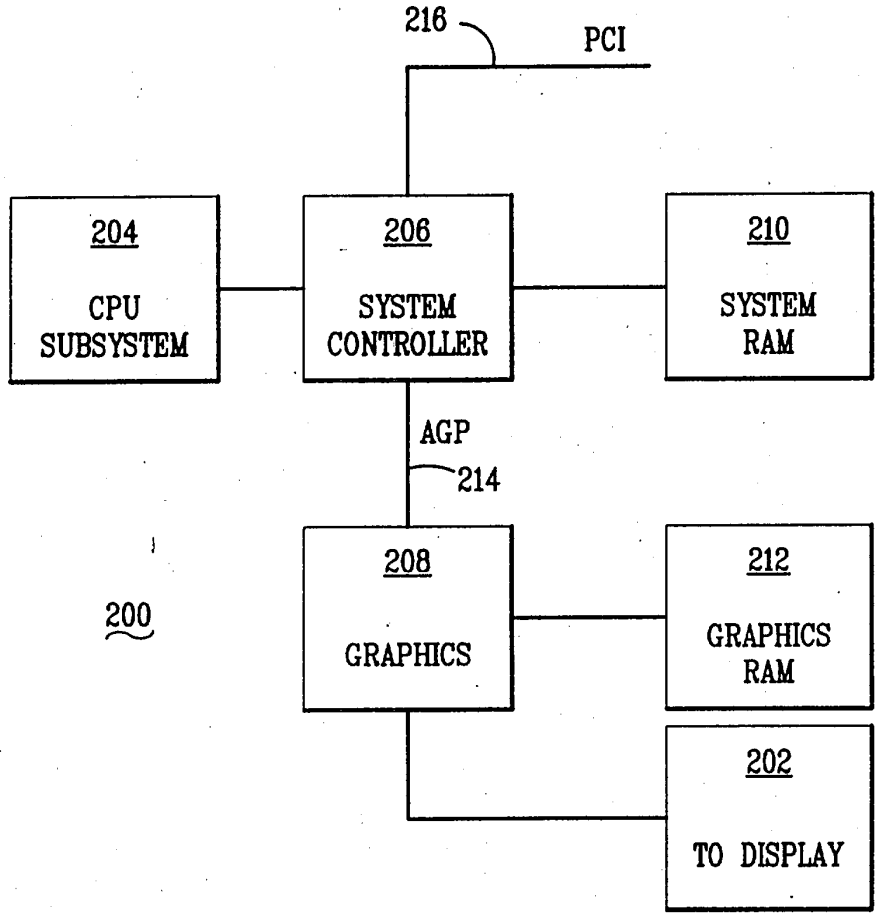

FIG. 2
Prior Art

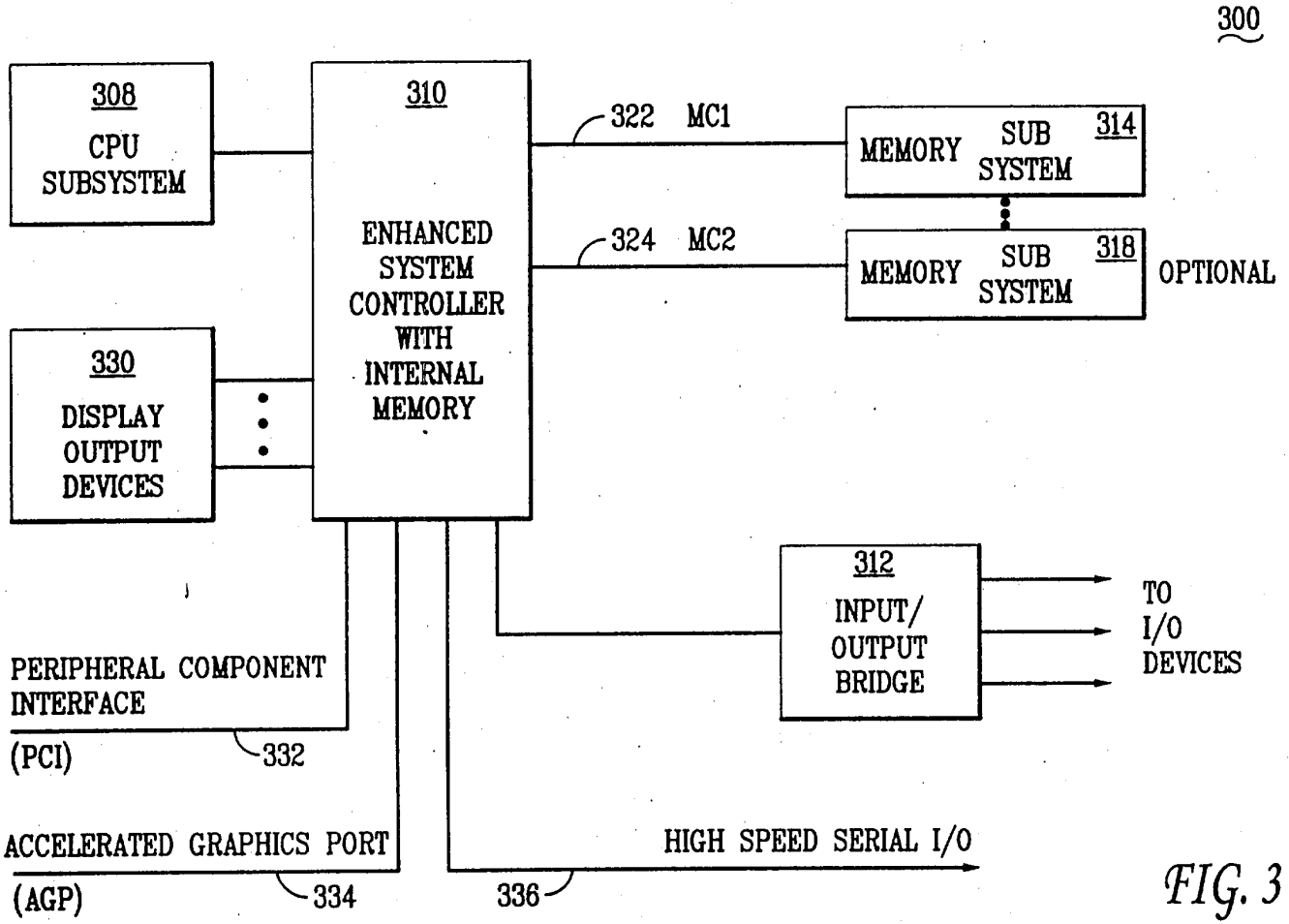
300
308
CPU SUBSYSTEM
310
ENHANCED SYSTEM CONTROLLER WITH INTERNAL MEMORY
322 MC1
324 MC2
MEMORY SUB SYSTEM 314
MEMORY SUB SYSTEM 318
OPTIONAL
330
DISPLAY OUTPUT DEVICES
312
INPUT/ OUTPUT BRIDGE
TO I/O DEVICES
PERIPHERAL COMPONENT INTERFACE
(PCI)
332
ACCELERATED GRAPHICS PORT
(AGP)
334
HIGH SPEED SERIAL I/O
336

FIG. 3

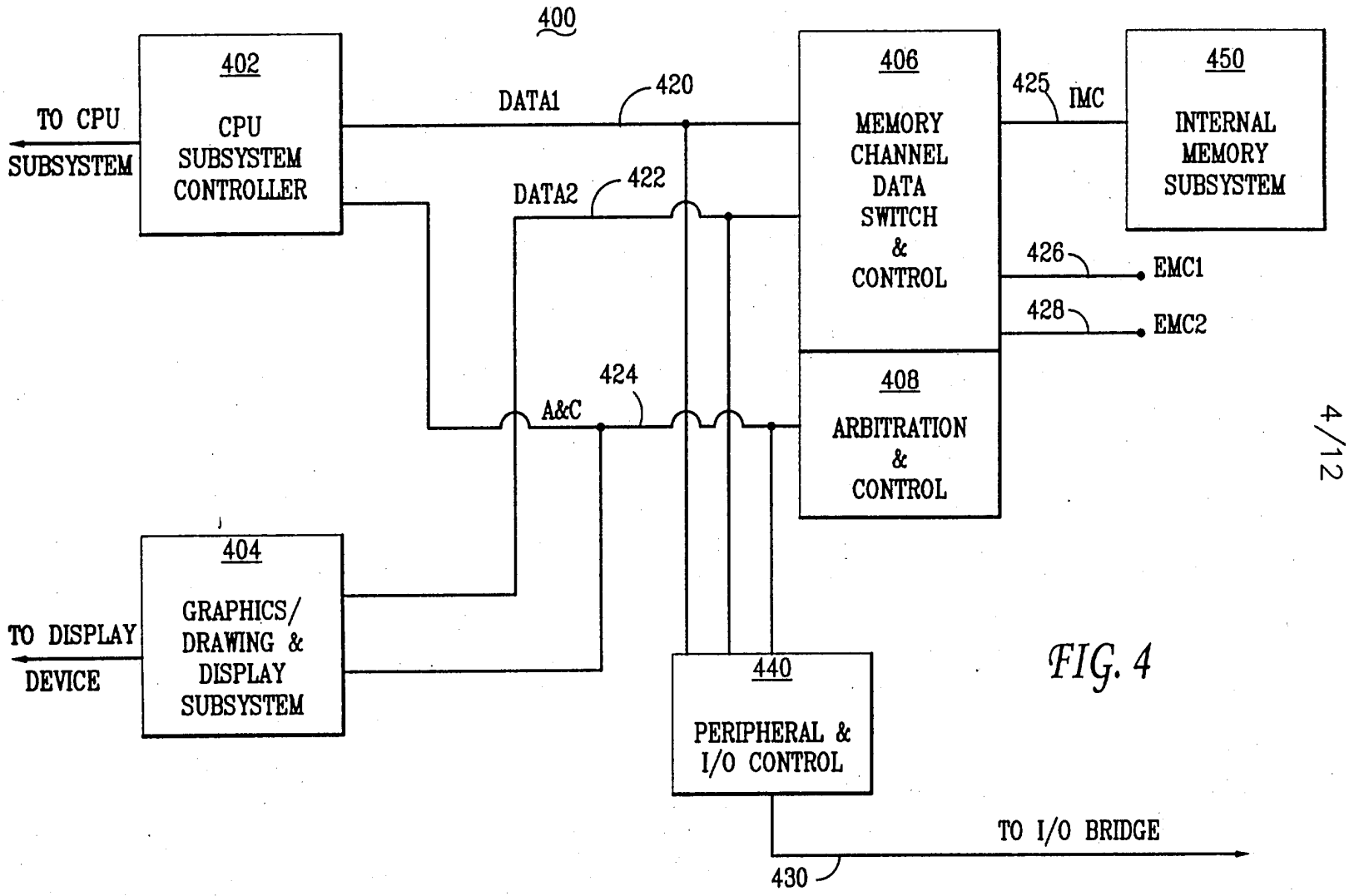
400
402
CPU SUBSYSTEM CONTROLLER
TO CPU SUBSYSTEM
DATA1
420
DATA2
422
406
MEMORY CHANNEL DATA SWITCH & CONTROL
425
IMC
450
INTERNAL MEMORY SUBSYSTEM
426
EMC1
428
EMC2
408
ARBITRATION & CONTROL
424
A&C
404
GRAPHICS/ DRAWING & DISPLAY SUBSYSTEM
TO DISPLAY DEVICE
440
PERIPHERAL & I/O CONTROL
TO I/O BRIDGE
430

FIG. 4

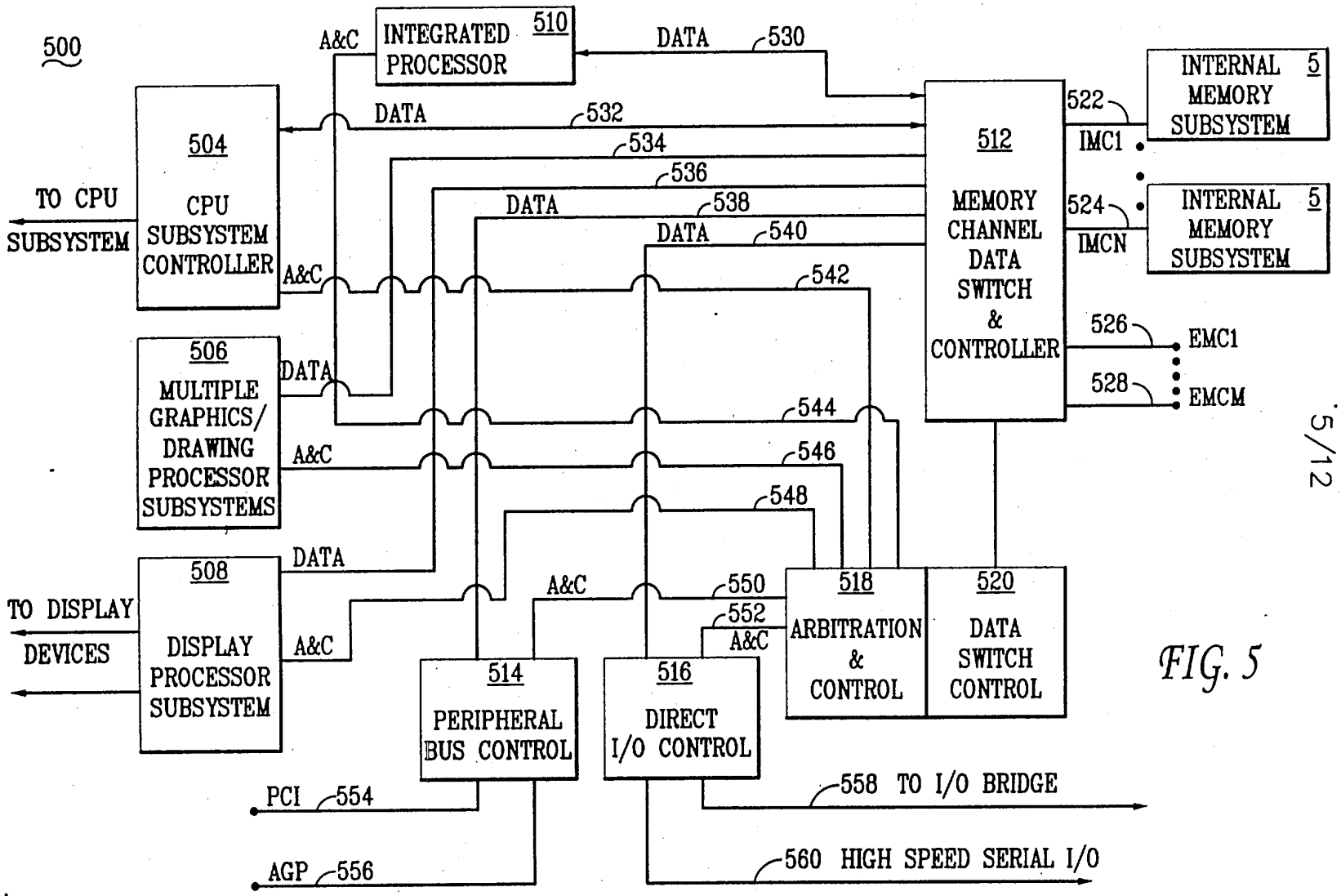
500
INTEGRATED PROCESSOR 510
A&C
DATA 530
504
CPU SUBSYSTEM CONTROLLER
TO CPU SUBSYSTEM
DATA 532
534
536
DATA 538
DATA 540
542
A&C
506
MULTIPLE GRAPHICS/ DRAWING PROCESSOR SUBSYSTEMS
DATA
544
A&C
546
548
508
DISPLAY PROCESSOR SUBSYSTEM
TO DISPLAY DEVICES
DATA
A&C
A&C
550
552
A&C
514
PERIPHERAL BUS CONTROL
516
DIRECT I/O CONTROL
518
ARBITRATION & CONTROL
520
DATA SWITCH CONTROL
512
MEMORY CHANNEL DATA SWITCH & CONTROLLER
522
IMC1
524
IMCN
INTERNAL MEMORY SUBSYSTEM 5
INTERNAL MEMORY SUBSYSTEM 5
526
EMC1
528
EMCM
PCI 554
AGP 556
558 TO I/O BRIDGE
560 HIGH SPEED SERIAL I/O

FIG. 5

5/12

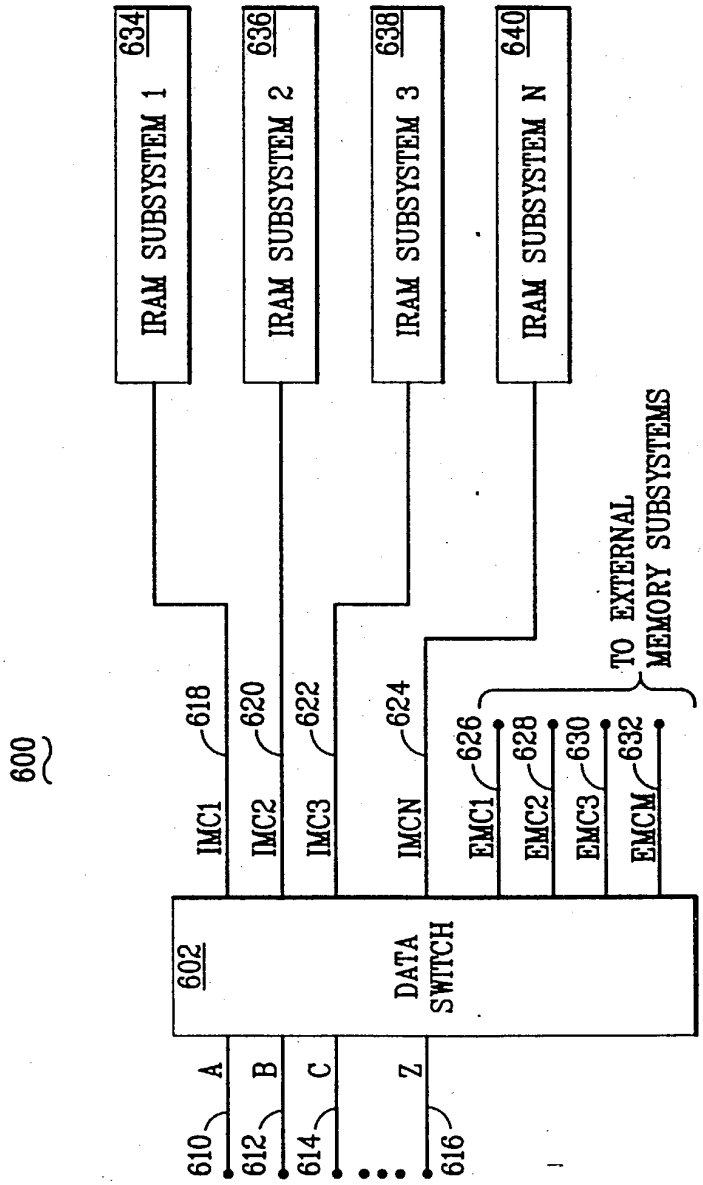
600
602
DATA SWITCH
IRAM SUBSYSTEM 1
634
IRAM SUBSYSTEM 2
636
IRAM SUBSYSTEM 3
638
IRAM SUBSYSTEM N
640
IMC1
618
IMC2
620
IMC3
622
IMCN
624
EMC1
626
EMC2
628
EMC3
630
EMCM
632
TO EXTERNAL MEMORY SUBSYSTEMS
A
B
C
Z
610
612
614
616
PROCESSING AND I/O DATA CHANNELS

FIG. 6

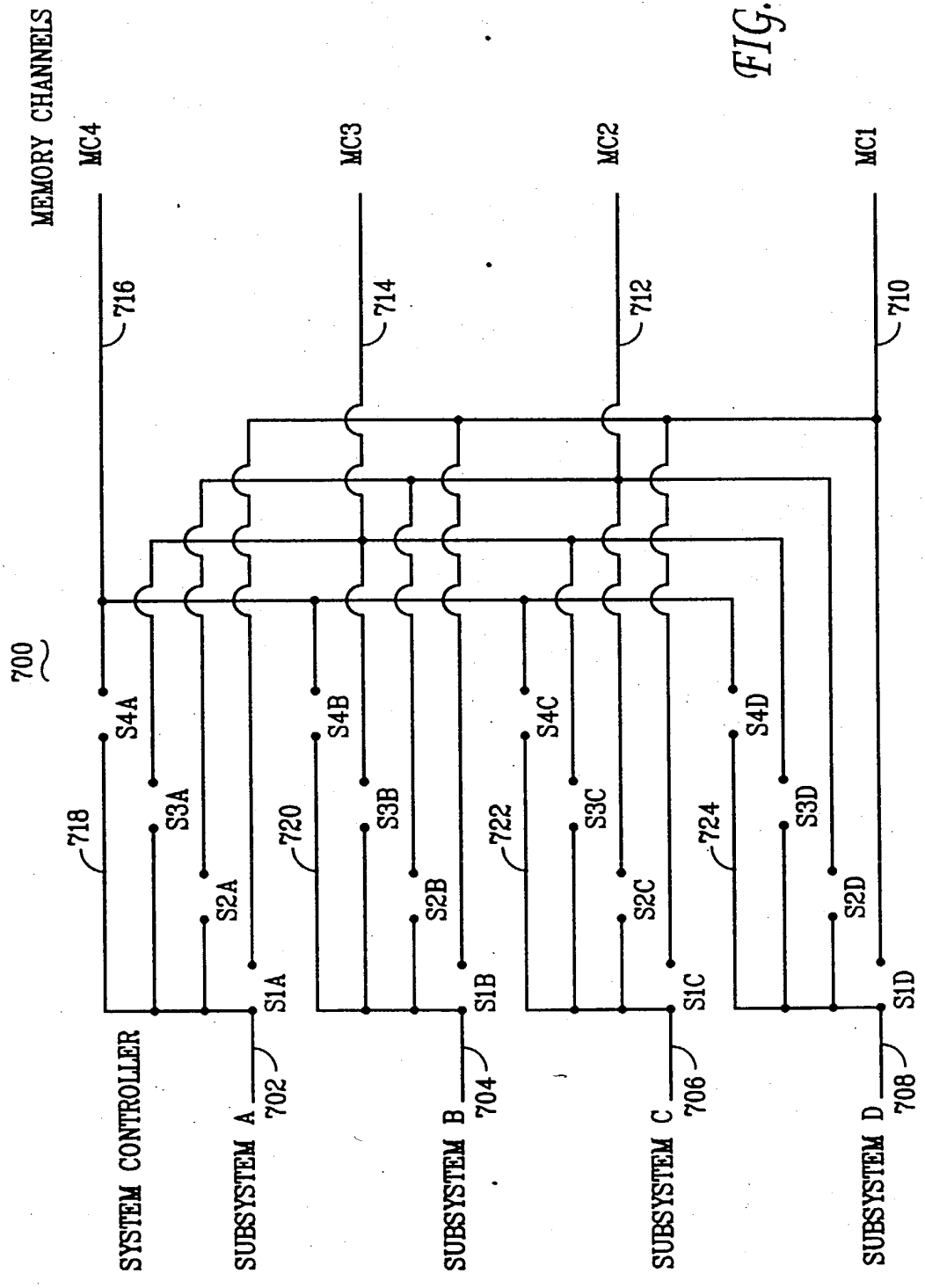
700
MEMORY CHANNELS
MC4
MC3
MC2
MC1
716
714
712
710
S4A
S3A
S2A
S1A
S4B
S3B
S2B
S1B
S4C
S3C
S2C
S1C
S4D
S3D
S2D
S1D
718
720
722
724
SYSTEM CONTROLLER
SUBSYSTEM A
SUBSYSTEM B
SUBSYSTEM C
SUBSYSTEM D
702
704
706
708

FIG. 7

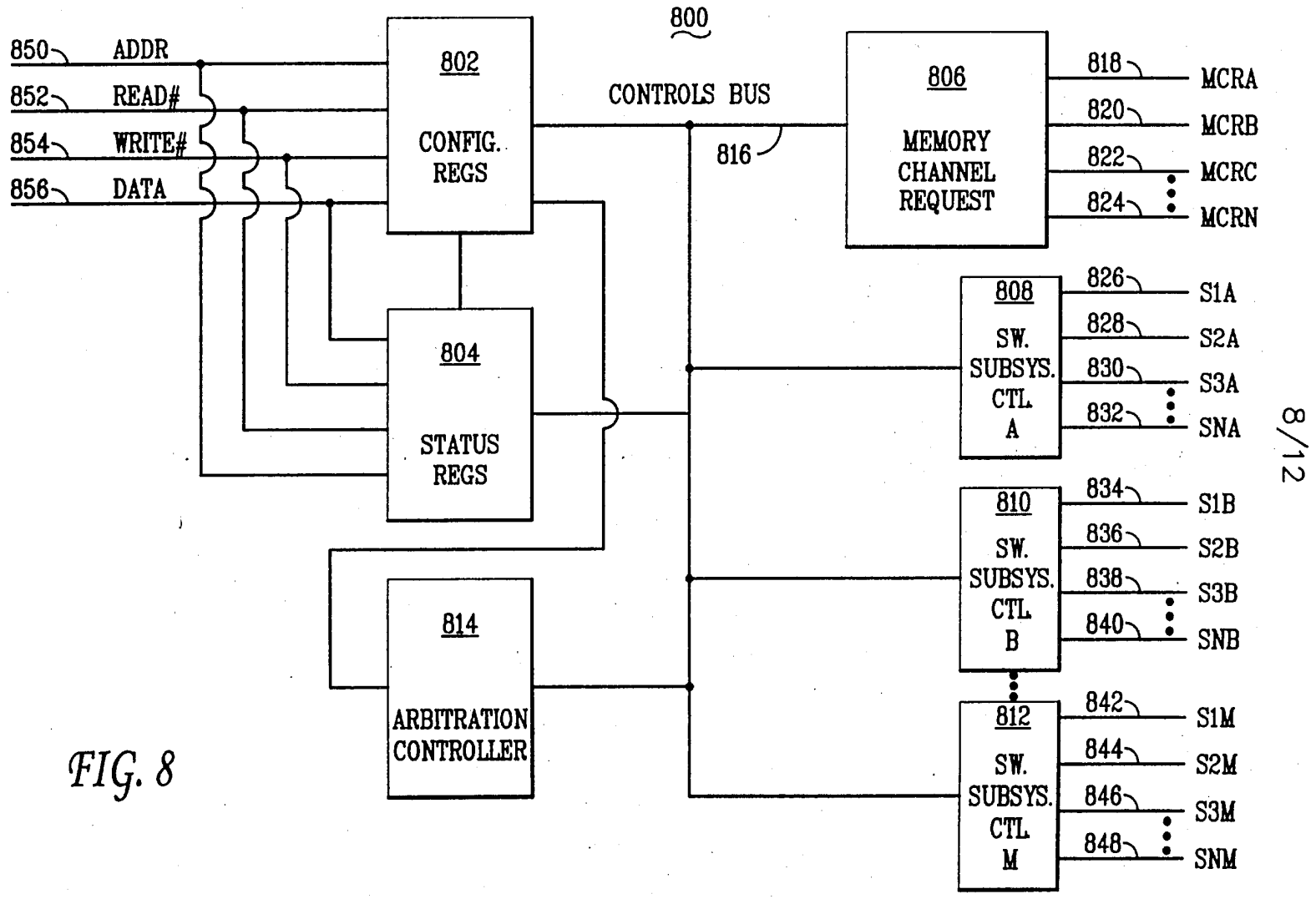
800
850 ADDR
852 READ#
854 WRITE#
856 DATA
802
CONFIG. REGS
804
STATUS REGS
814
ARBITRATION CONTROLLER
CONTROLS BUS
816
806
MEMORY CHANNEL REQUEST
818 MCRA
820 MCRB
822 MCRC
824 MCRN
808
SW. SUBSYS. CTL. A
826 S1A
828 S2A
830 S3A
832 SNA
810
SW. SUBSYS. CTL. B
834 S1B
836 S2B
838 S3B
840 SNB
812
SW. SUBSYS. CTL. M
842 S1M
844 S2M
846 S3M
848 SNM

FIG. 8

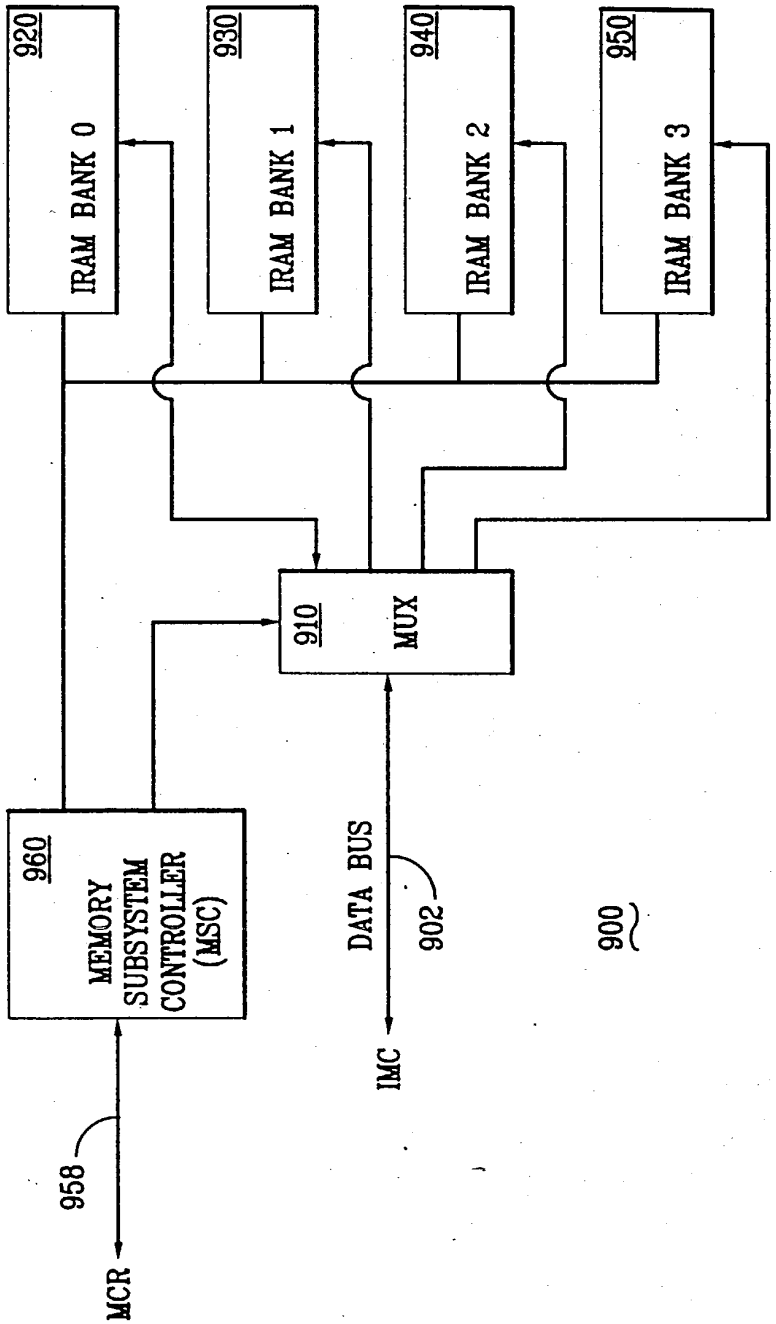
920
IRAM BANK 0
930
IRAM BANK 1
940
IRAM BANK 2
950
IRAM BANK 3
910
MUX
960
MEMORY SUBSYSTEM CONTROLLER (MSC)
DATA BUS
902
900
958
MCR
IMC

FIG. 9

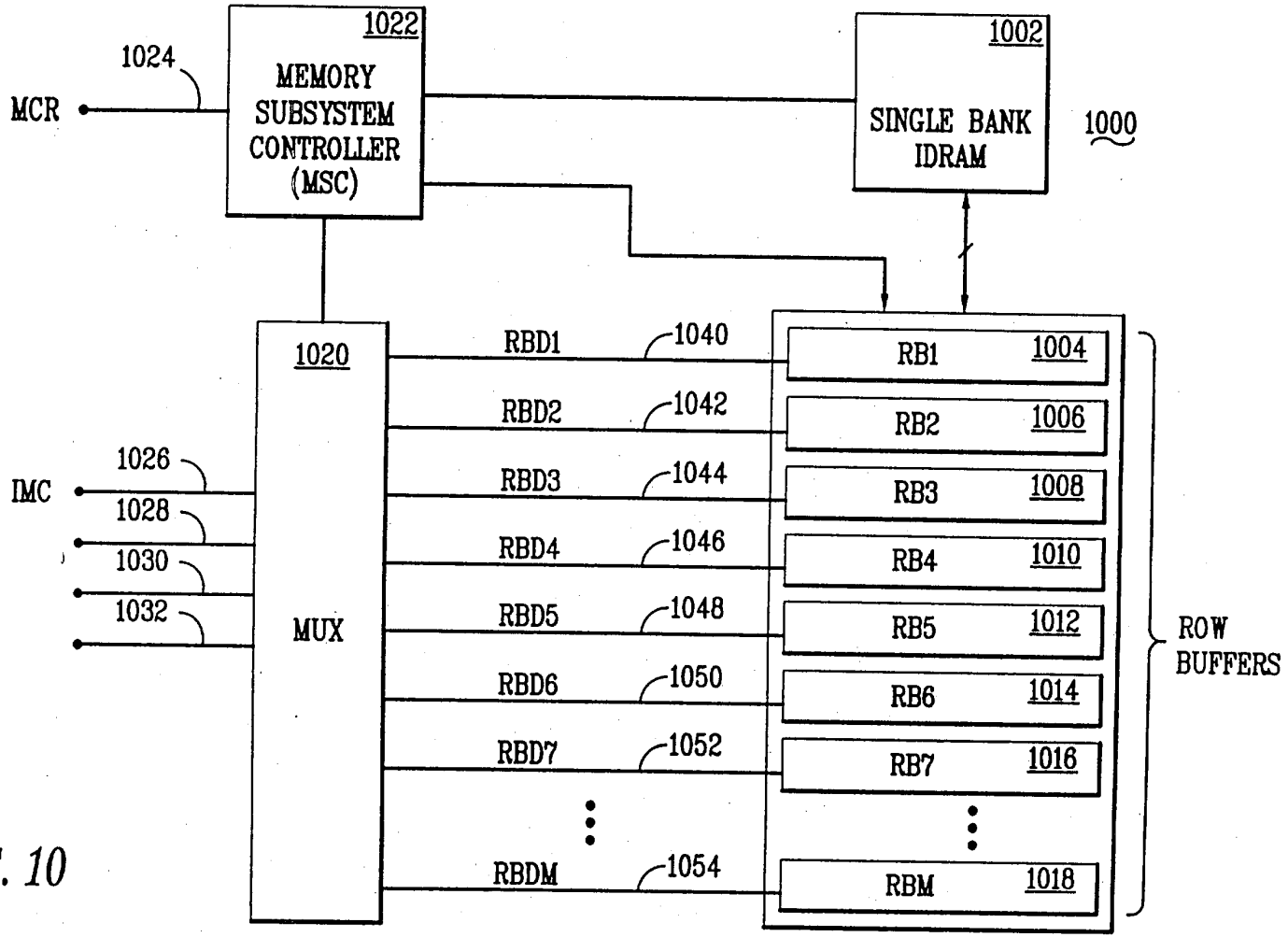
1022
MEMORY SUBSYSTEM CONTROLLER (MSC)
1024
MCR
1002
SINGLE BANK IDRAM
1000
1020
MUX
1026
IMC
1028
1030
1032
RBD1
1040
RBD2
1042
RBD3
1044
RBD4
1046
RBD5
1048
RBD6
1050
RBD7
1052
RBDM
1054
RB1
1004
RB2
1006
RB3
1008
RB4
1010
RB5
1012
RB6
1014
RB7
1016
RBM
1018
ROW BUFFERS

FIG. 10

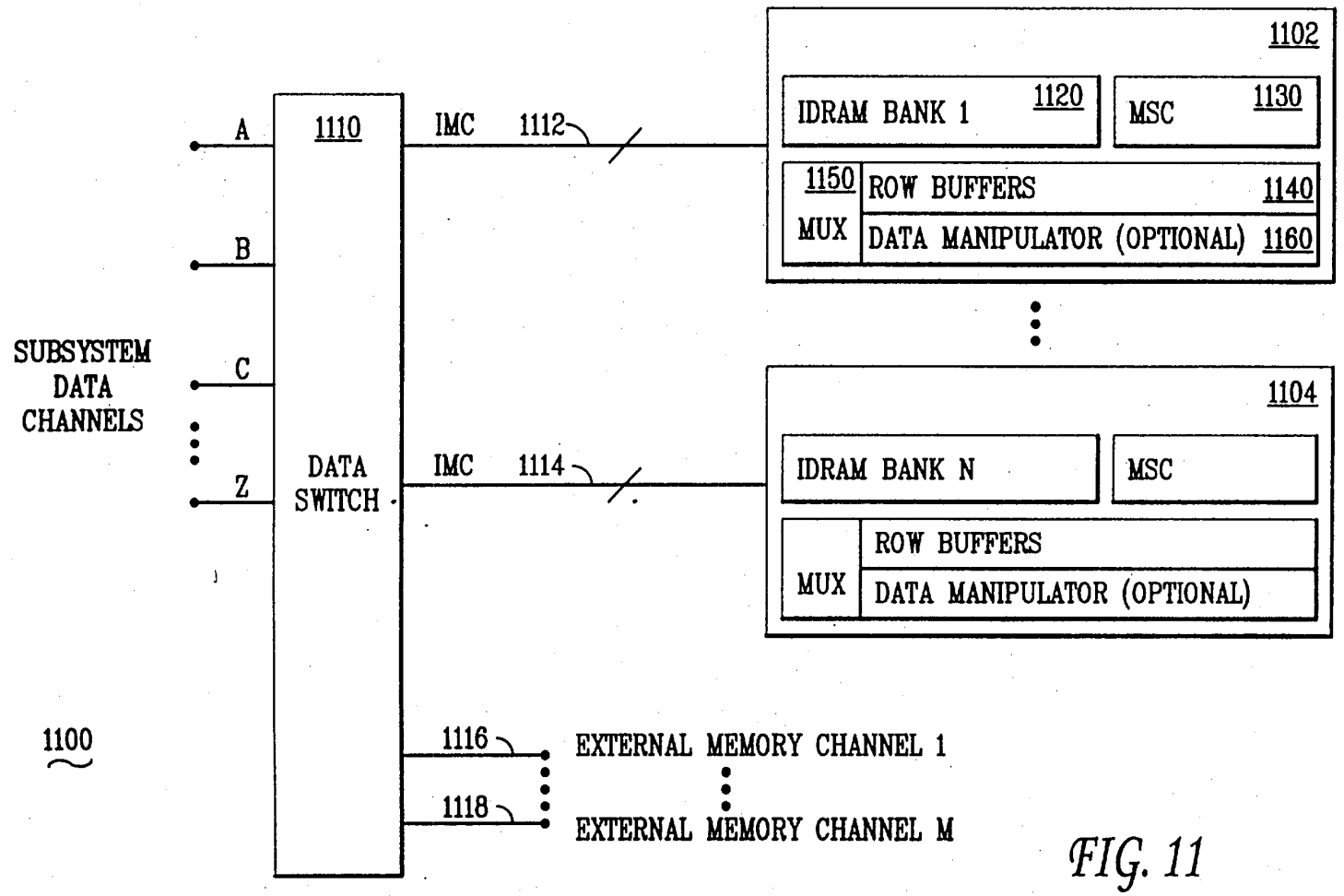
1102
IDRAM BANK 1
1120
MSC
1130
1150
MUX
ROW BUFFERS
1140
DATA MANIPULATOR (OPTIONAL)
1160
1104
IDRAM BANK N
MSC
MUX
ROW BUFFERS
DATA MANIPULATOR (OPTIONAL)
SUBSYSTEM DATA CHANNELS
A
B
C
Z
1110
DATA SWITCH
IMC
1112
IMC
1114
1100
1116
1118
EXTERNAL MEMORY CHANNEL 1
EXTERNAL MEMORY CHANNEL M

FIG. 11

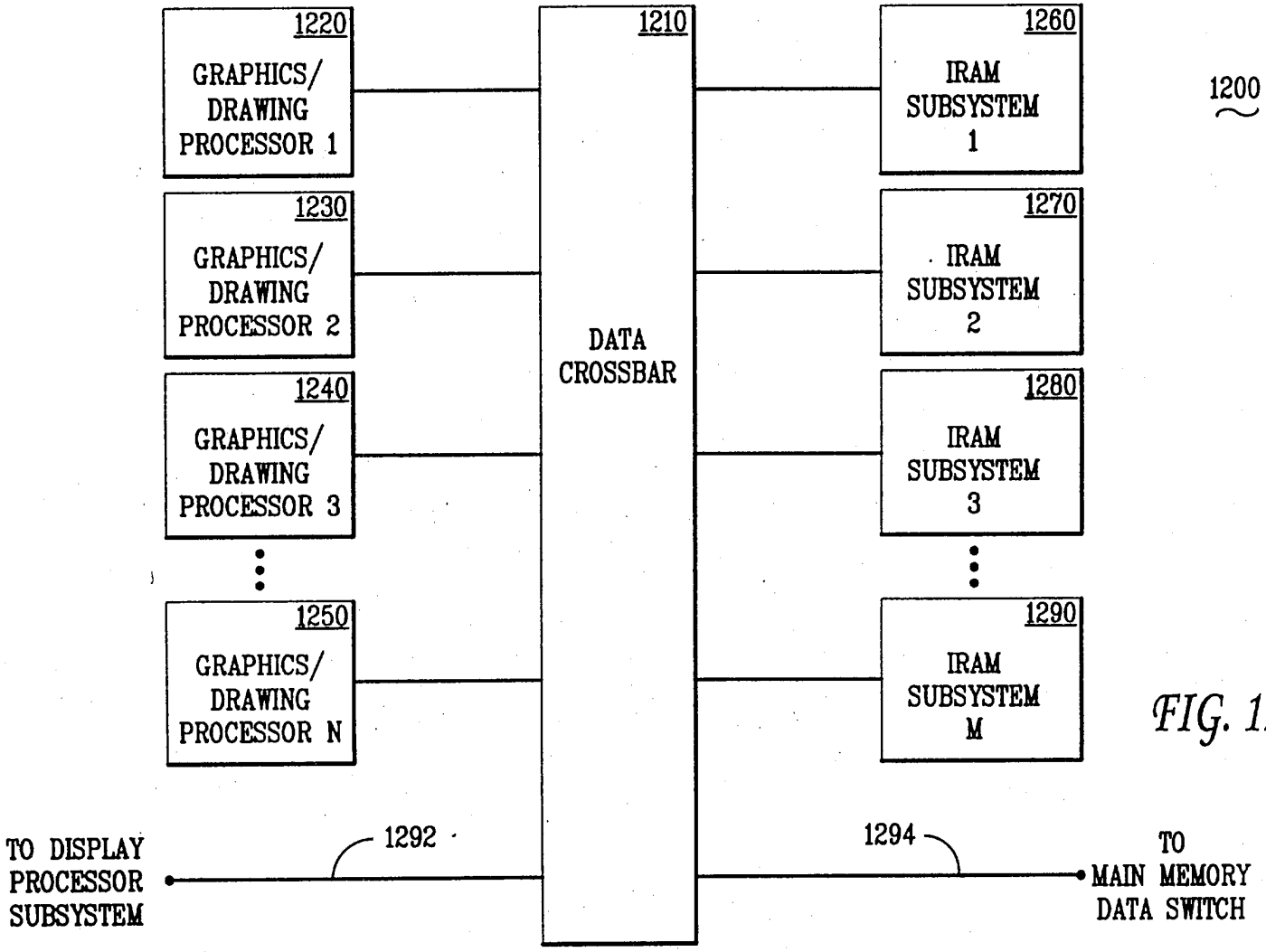
1220
GRAPHICS/ DRAWING PROCESSOR 1
1230
GRAPHICS/ DRAWING PROCESSOR 2
1240
GRAPHICS/ DRAWING PROCESSOR 3
1250
GRAPHICS/ DRAWING PROCESSOR N
1210
DATA CROSSBAR
1260
IRAM SUBSYSTEM 1
1270
IRAM SUBSYSTEM 2
1280
IRAM SUBSYSTEM 3
1290
IRAM SUBSYSTEM M
1200
1292
TO DISPLAY PROCESSOR SUBSYSTEM
1294
TO MAIN MEMORY DATA SWITCH

FIG. 12